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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,062	04/28/2005	Tadaaki Tanimoto	TAM-104	3125

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EXAMINER	
SANDOVAL, PATRICK	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,062	TANIMOTO ET AL.	
	Examiner	Art Unit	
	PATRICK SANDOVAL	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Final Office Action responds to Applicant's amendment filed 12/22/2009. Claims 1 and 6 have been amended. Claims 1 and 6 are pending.

Response to Arguments

2. Applicant's arguments and claim amendments, see Remarks Pages 5-6, filed 12/22/2009, ***with respect to the rejection(s) of claim(s) 1 and 6*** under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

3. However, upon further consideration, a new ground(s) of rejection is made in view of newly discovered prior art reference **Dietz**, H.G. (Dietz) "Meta-State conversion", Purdue Libraries ECE Technical Supports, TR-EE 93-6, Janurary 1993, previously applied prior art reference **Panchul** et al. (US2001/0034876) and previously applied IDS reference **Nakata** et al. (Nakata), "Deriving Parameter Conditions for Periodic Timed Automata Satisfying Real-Time Temporal Logic Formulas", Proc. of IFIP TCPfWG6. 1 Int. Conf. on Formal Techniques for Networked and Distributed Systems (FORTE2001),Kluwer Academic Publishers, 2001.08, pages 151-166.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1 and 6 are rejected** under 35 U.S.C. 103(a) as being unpatentable over **Dietz**, H.G. (Dietz) "Meta-State conversion", Purdue Libraries ECE Technical Supports, TR-EE 93-6, Janurary 1993 in view of **Panchul** et al. (US2001/0034876), further in view of **Nakata**, et al., (Nakata), "Deriving Parameter Conditions for Periodic Timed Automata Satisfying Real-Time Temporal Logic Formulas", Proc. of IFIP TCP/WG6. 1 Int. Conf. on Formal Techniques for Networked and Distributed Systems (FORTE2001), Kluwer Academic Publishers, 2001.08, pages 151-166.

6. **Pursuant to claims 1 and 6**, Dietz discloses an algorithm for meta-state conversion of a multiple instruction stream, multiple data stream (MIMD) program comprising:

inputting program descriptions which define a plurality of devices by employing a program language capable of describing parallel operations (Dietz, Page 17, Section 4.1, input language is a parallel dialect of C called MIMDC, Page 2, Section 1, introduction, Pages 14-15, Sections 3-3.1, execution of different operations in parallel);

converting the input program descriptions into an intermediate expression (Dietz, Page 3, Section 1.2, conversion of multiple instruction stream, multiple data stream (MIMD) program into an automaton based on meta states);

real-time restrictions, for the intermediate expression (Dietz, Page 4, Section 2, conditional operation such as in Listing 1, Page 5-6, Section 2.2, targets known at runtime, Page 16, Section 3.2.4, adjustment of multiple exit arcs if some but not all processing elements have reached a barrier at time of meta state execution completion;

wherein for example processing elements are allowed to set their process counter (pc) values to 9 but are not permitted to enter meta state 9 unless all pc's are 9);

synthesizing circuit descriptions which are based on a hardware description language, on the basis of the generated parameters (Dietz, Abstract and Page 1, Section 1, introduction, duplication of MIMD execution using SIMD hardware, Page 4, Section 2, algorithm for conversion to meta-state automaton, Page 14, Section 3, coding and implementation of VLIW execution structures on SIMD hardware, Page 16, Section 3.2.5, restricted form of dynamic process creation);

wherein the program descriptions define the devices on a single bus by using a run method of the program language and define clock synchronizations of the device by using barrier synchronizations (Dietz, Page 13, Section 2.6, barrier synchronization);

wherein in the run method, program codes which are to be executed in a thread constituting a multi-thread are described (Dietz, Pages 14-15, Section 3.1, wherein meta-state automaton coding, a common subexpression induction (CSI) algorithm analyzes a segment of code containing operations executed by any of multiple threads); and

imposing an inhibition of dynamic instantiation restriction (Dietz, Page 16, Section 3.25, restricted dynamic process creation) and an inhibition of a start method call from the run method restriction on the program descriptions (Dietz, Page 4, Section 2, meta-state conversion with regards to MIMD start states, Pages 6-7, Section 2.3, base algorithm for meta-state conversion with regards to start states);

wherein the intermediate expression comprises a temporal automaton (Dietz, Page 11, Section 2.5 meta state compression resulting in created automata) and a concurrent control flag generated by expressing the start of the "synchronized" operation as a node which is labeled as "Begin sync" and the end thereof as a node which is labeled as "End sync", (Dietz, Pages 13-14, Section 2.6, barrier synchronization for state space reduction without adding to complexity of meta states, Page 14, section 3, SIMD coding of meta-state automaton, Page 16, Section 3.2.4, treatment of exit arcs with regards to whether or not processing elements have reached a barrier at the time a meta state's execution completes); and

wherein the temporal automaton is converted from the concurrent control flow flag in which a part held between description the "Begin sync" and the "End sync" are identified, and is set as a "sync" block, a clock boundary node which does not exist in the "sync" block is set as a state allotment candidate, and (Dietz, Page 4, Section 2, meta-state conversion algorithm wherein code for MIMD processes is converted into a set of control flow graphs in which each node (MIMD state) represents a basic block, wherein a set of MIMD start states form the start state of a meta-state automaton, Page 5, Section 2.1, program code is converted to traditional control-flow graph form to facilitate analysis for meta-state conversion, Page 13, Section 2.6, barrier synchronization, barrier prevented transitions past an MIMD state; wherein MIMD barrier wait states are constructed for components to wait at).

7. Dietz does not disclose:

Defining devices by employing a program language such as a Java program language; and

generating parameters which satisfy a real-time restriction, wherein parametric model checking is performed for the parameter generation.

8. Panchul discloses algorithmic representation of preliminary hardware design in high-level language such as Java (Panchul, Paragraphs 22, 112) with parallel processing of functions (Panchul, Paragraphs 62-63, 152).

9. Nakata discloses a symbolic model checking method for parametric periodic timed automata (Nakata, Abstract, Section 2, parametric and periodic timed automata) as a useful and effective method for reliable hardware/software system design (Nakata, Section 1, Introduction, first paragraph), wherein an algorithm is utilized for deriving parameters for a timed automaton model which satisfies a formula of a real-time extension of CTL (Nakata, Section 1, Introduction, fourth paragraph, Section 3, Real-time CTL).

10. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to substitute any standard C-type programming language such as Java, ANSI C, C++, etc. with the high-level language as taught by Dietz for flexibility amongst designers/programmers.

11. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention that the teachings of Nakata for "on-the-fly" model checking used in the design of reliable hardware/software systems allows for reduction of computation complexity in model checking, thus providing time and processing power savings

(Nakata, Section 1, introduction, fourth paragraph, Section 4.2, first paragraph, Section 5, first paragraph).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICK SANDOVAL whose telephone number is (571)272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Patrick Sandoval/
Examiner, Art Unit 2825

/Vuthe Siek/
Primary Examiner, Art Unit 2825